ABSTRACT OF THE DISCLOSURE

The invention provides a semiconductor device that allows high-scale integration of a pattern layout to reduce the pitch of wiring lines without changing a design rule, and to provide an electro-optical unit and an electronic apparatus including the semiconductor device. The semiconductor device can include a substrate, which has the following layers thereon: in order, a first conductive layer, an insulating interlayer having a contact hole therein at a position where it overlaps the first conductive layer in plan view, and a second conductive layer electrically connected to the first conductive layer via the contact hole. The first conductive layer entirely overlaps the contact hole, while the second conductive layer partially overlaps the contact hole in plan view. The first conductive layer is in contact with the second conductive layer at a part of a bottom area of the contact hole.